CURRICULUM VITAE

Georgios Dimitriou

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EDUCATION:

- Undergraduate studies: Diploma of Electrical Engineering, Department of Electrical Engineering, National Technical University of Athens (1983-1988). Diploma grade: 9,55/10.
- Postgraduate studies: Master of Science (MS) and Doctor of Philosophy (PhD) degrees, Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, Illinois, USA (1989-2000).

WORK:

- Monthly summer work within a program of IAESTE (International Association for the Exchange of Students for Technical Experience) at the Institute for Physical Research (KFKI) of Budapest (Summer 1987). Subject: Digital filter programming for applications in physics.
- One-semester research work, concurrently with a teaching appointment (as lab supervisor and grader) in a parallel processing laboratory, at the Computer Science Division of the Department of Electrical Engineering of the National Technical University of Athens (NTUA) (Spring 1989).
- Research assistant at the University of Illinois at Urbana-Champaign (UIUC), USA, and in particular, at the Center for Supercomputing Research and Development (CSRD). More specifically: Between September 1989 and May 1996 my research subject was task and thread scheduling in operating systems, completed with the three-month summer work mentioned below. Between January 1997 and May 2000 my research subject was multithreaded processor architecture and code generation for such processors, completed with my doctoral dissertation.
- Teaching assistant at UIUC, and in particular at the Department of Electrical and Computer Engineering, in a postgraduate course on Computer Architecture (Fall 1996).
- Three-month summer internship at Silicon Graphics, Inc. (SGI), Mountain View, California, USA (Summer 1996).
- Visiting teaching staff (on a per semester contract basis) at the Department of Electrical and Computer Engineering (ECE, previously Department of Computer and Communication Engineering – CCE) of the University of Thessaly (UTH) (Academic periods from fall 2001 semester until spring 2017 semester – four autonomous and other co-taught courses).
- Visiting teaching staff (on a per semester contract basis) at the Department of Computer Science (CS) of UTH (Academic periods from fall 2013 semester until spring 2017 semester – three autonomous and one co-taught course).

- Visiting teaching staff at the graduate programs of the ECE and CS departments of UTH (Academic periods from fall 2013 semester until spring 2017 semester – four autonomous and one co-taught course).
- Participation in the research project of CERTH-IRETETH «NANOTRIM- Continuous Transistor Sizing Toolset for nanoscale IC optimization» (February 2014 - October 2015).
- Since October 2017, appointed faculty at the CS department of UTH, as an Assistant Professor, in the field of "Parallel Computer Architectures".
- Since September 2019, elected director of the newly established Laboratory for Computer Architecture, Compilers and System Security, in the Department of Computer Science and Telecommunications (CST, prior CS) of the UTH for three years.

RESEARCH ACTIVITY - RELATED PUBLICATIONS:

1. **Parallel programming in Transputer networks** (NTUA – Diploma thesis, Research work)
   Short description: Transputer was the first European microprocessor for parallel processing in the decade of 1980. The uniqueness of its organization was mainly due to the presence of multiprogramming capabilities in hardware, and through its four communication channels it could be directly connected to other Transputers. We developed two concurrent applications for Transputer networks, using the Occam parallel programming language: A hierarchical digital image boundary detection algorithm based on graph theoretic techniques (diploma thesis) and a parallel attribute grammar evaluator for the representation and processing of knowledge (research work). Both applications were tested on various Transputer network topologies. [A1][B1]
   Spring 1988 - Spring 1989.
2. **Simulation of Static and Dynamic Task Scheduling on Multiprocessor Systems** (CSRD – MS thesis)
   Short description: Finding an optimal task schedule for a parallel job on a multiprocessor is a problem that is approached either statically – through the compiler, or dynamically – through a run-time scheduler. In this work, we compare and evaluate the performance of several scheduling algorithms in a simulated parallel processing environment. Given a parallel job represented as a hierarchical task graph, we transform it into an intermediate form and then feed this form into the simulated architecture to execute it. Several heuristic scheduling algorithms were developed as part of this work, which are hybrids between static and dynamic algorithms. [MSThesis]
   Fall 1989 - Spring 1994.
3. **nanoThreads: A User-level Multithreading Library** (CSRD, and SGI summer internship)
   Short description: Cooperation of the compiler and the operating system in the exploitation of parallelism through multithreading is essential for the minimization of overhead incurred by the handling of threads. Ultra-lightweight threads can be created through library calls at user level, within user space, with only minimal interaction with the operating system, which provides the execution vehicles – i.e. the processors – at system level. This minimization of interaction between user and system level is the main focus of this work. The multithreading library developed is called nanoThreads and has been implemented for SGI's IRIX systems.
   Fall 1994 - Spring 1996 (CSRD), Summer 1996 (SGI).
4. **Loop Scheduling for Multithreaded Processors** (CSRD – PhD thesis)
   Short description: The presence of multiple active threads on the same processor affects the performance of existing loop scheduling techniques significantly. We introduce a loop-scheduling technique for multithreaded processors that we call Macro-Software

Pipelining (MSWP), which produces loop schedules by partitioning the loop body into tasks and assigning each task to a processor thread that executes all loop iterations for that task. MSWP is applied on a hierarchical representation of a program code and utilizes task-level speculation for maximal exploitation of parallelism. We study the application of MSWP on our architectural model, Coral 2000, a novel hybrid between blocked and interleaved multithreaded architectures. We tested MSWP on a Coral 2000 simulator, using several synthetic and SPEC benchmarks with encouraging results that reached speedups of up to 30% with respect to highly optimized schedules. [PhDThesis][B2][B3]
Spring 1997 - Spring 2000.

5. **Dissipated power estimation in wireless sensor networks** (UTH)
Short description: Power and total useful lifetime are primary design concerns of fundamental importance, in a variety of real life applications, where the deployment of a Wireless Sensor Network is desired. This work focused on the design and implementation of a tool to calculate power consumption in wireless sensor networks. Power consumption is calculated on the execution of C programs on a simulator, and the tool is based on a C interpreter developed from scratch within this work. The methodology used in order to estimate power consumption is based on a number of user-defined parameters. [B4]
Spring 2004 - Spring 2005.

6. **"NoFun" microprocessor core architecture** (UTH)
Short description: Multithreaded multicore processors are the state-of-the-art in microprocessor technology. In this project, we are exploring the NoFun processor design, in which multiple single-threaded pipelines meet at a unified out-of-order back-end. In that back-end, key role plays a Network of Functional unit nodes, able to execute instructions from any one of the active pipelines of the processor. Goal of this project is to achieve a speedup in loop execution proportional to the network size, regardless of the number of cores and threads, and at the same time a substantial decrease in power consumption. Within the NoFun project, new techniques in compilation and on-chip interconnection are designed and implemented, with significant preliminary results. [A2][B5][B20]
Fall 2012 - today.

7. **Adding a C front end to the "CCC" high-level synthesis tool** (UTH, TEI of Kastoria)
Short description: High level synthesis is developing into the dominant technique to design ICs. CCC is a high level synthesis tool translating ADA into synthesizable HDL, using logic programming, in order to make translation self-proven. The C compiler front end provides the tool with the ability to accept C programs, translating them into ADA. Restrictions on the C input language are kept minimal, while restrictions on the ADA code are invisible to the programmer. A number of compilation options allow a better match between C and ADA programs. [A3][A4][B6][B12] [B13][B17][B21]
Fall 2013 - October 2015.

8. **Participation in the "Nanotrim" research project** (CERTH-IRETETH)
Short description: Intervention in the predefined transistor sizes of CAD tool output files for integrated circuit design. Using a careful theoretical analysis, we calculate the sizes that lead to a better performance with regard to both time and energy. The files are modified in such a way that overall performance is enhanced, without affecting the circuit functionality. Main participation in file manipulation, and in particular in parsing as a preprocessing step for the aforementioned intervention. [B7][B8][B9][B10] [B11][B14][B15][B16][B18][B19][B23][B29][B31]
February 2014 - October 2015.

9. **Studying and implementing optimization techniques in the front-end intermediate representation of the "CCC" tool** (UTH, TEI of Kastoria)

Short description: Optimization through source code transformations is quite different from optimization at the back-end scheduler of a high-level synthesis tool. After the C source code is turned into an ast-based intermediate representation, several high-level transformations, e.g loop unrolling, loop pipelining, code motion, function inlining, are applied on the representation, giving an optimized ADA code, which is then fed into CCC. Thus, the back end is only concerned with hardware scheduling, to deliver a doubly optimal synthesizable HDL code. [B22][B24][B25][B26][B27][B28]
October 2015 - today.

10. **Issues on the education of computer science** (UTH)
    Short description: The education of computer science in schools exhibits many challenges to the teachers. Some issues are attempted to be solved through specialized programming, like programming in asynchronous learning platforms. [B30]
    Fall 2017 - today.
11. **Timing analysis in microprocessor circuits** (UTH)
    Short description: Timing analysis in microprocessor circuits is more efficient when architectural constraints are introduced, allowing a better-than-worst-case design. New timing analysis algorithms are explored, and utilized for timing speculation without the need for expensive error correction mechanisms. [B32][B33]
    Spring 2018 - today.

RESEARCH INTERESTS:

- Computer architecture (general-purpose microprocessors, instruction-level parallelism, dynamic instruction scheduling, speculative execution, multithreading, parallel processing, special-purpose microprocessors – multimedia, graphics, network and signal, microcontrollers, systems-on-a-chip, chip multiprocessors, multicore architectures, edge architectures, accelerators, big-data architectures).
- Compilers (optimizations, syntax trees, register allocation, code generation, instruction and loop scheduling, code parallelization, compiler construction tools, high-level programming languages, machine languages, hardware description languages, high-level synthesis).

TEACHING:

- Teaching assistant at NTUA: One semester work for an undergraduate laboratory course on Parallel Processing, the main tools for which were Transputer nodes. Assistance in terms of laboratory supervision and exercise grading (Spring 1989).
- Teaching assistant at UIUC: One semester work for a postgraduate course on Computer Architecture. Assistance in terms of teaching in the absence of the instructor, project supervision and homework grading (Fall 1996).
- Visiting teaching staff or appointed faculty at UTH.
  Autonomous courses:
  1. **Computer Organization** (mandatory course). (Fall 2001 semester and all spring semesters between 2002 and 2013, CCE/ECE, all fall semesters between 2014 and 2018, CS).
  2. **Computer Architecture** (elective course). (All fall semesters between 2003 and 2017, CCE/ECE, fall semester 2018, CS).
  3. Computer Architecture (same as above #2, in the graduate program). (Fall semesters of 2006, 2011, and all fall semesters between 2013 and 2017, CCE/ECE).
  4. **Computer Organization and Design** (in the graduate program). (Spring semesters 2016, 2017 and 2018, CCE/ECE).

5. **Languages and Translators** (mandatory course). (All fall semesters between 2002 and 2013, CCE/ECE).
6. Compilers (mandatory course, same as above #5). (All fall semesters between 2015 and 2018, CS).
7. Compilers (elective course, same as above #5). (All fall semesters between 2014 and 2018, ECE).
8. **Introduction to Computers** (mandatory course). (All spring semesters between 2014 and 2019, CS).
9. **Advanced Topics on Compilers** (elective course). (All spring semesters between 2014 and 2018, ECE).
10. Advanced Topics on Compilers (same as above #9, in the graduate program). (All spring semesters between 2014 and 2018, ECE).
11. **Software Development and Design** (in the graduate program). (All spring semesters between 2016 and 2019, CS).
12. **Parallel Systems** (elective course). (All spring semesters between 2017 and 2019, CS).

Courses co-taught:

13. **Digital Design I** (mandatory course, the laboratory part). (Fall 2001 semester, CCE).
14. **Digital Design II** (mandatory course, the laboratory part). (Spring 2002 semester, CCE).
15. **Introduction to Programming** (mandatory course, the laboratory part). (Fall 2013 semester, CS).
16. Software Development and Design (part of the above #11). (Spring 2015 semester, CS).

For all above courses, hundreds of pages of original examples and exercises were written, and several different projects were given.

OTHER ACADEMIC WORK:

- Participation in international conferences, where the above research work has been presented
- Supervision of several diploma theses, both undergraduate and postgraduate, in the CCE/ECE and the CS departments; representative are
  - G.Drasidis, “Study of dual-core processors, cache coherence protocols and implementation on an FPGA”, 2008.
  - St.Alhatzidis, “Graphical representation, processing and simulation of abstract syntax trees”, 2008.
  - I.Arvanitakis, D.Mamalis, “Study of replacing the core of the Leon3 processor from SPARC into MIPS architecture”, 2010. Presented in SFHMMY 2010.
  - P.Chalkias, Ar.Iakovou, M.Prodromou, K.Roumeliotou, “Automatic transistor modification at the physical level”, 2011.
  - El.Voumvourakis, “Integrated system of a wireless sensor network for the monitoring of environmental conditions and their depiction on GIS”, 2011.
  - At.Tziouvaras, “Fast, low-power loop execution in a network of functional units”, 2013.
  - Kl.Kalaitzidis, “Power consumption simulation of a multiple functional unit processor based on the tools Simplescalar and Wattch”, 2014.
  - At.Tziouvaras (graduate), “Memory hierarchy issues in processing large data sheets”, 2015.
  - G.Chatzianastasiou, Ap.Tsakyridis, “Implementation of optimizing transformations in a high-level synthesis compiler”, 2016.

- D.Varsos (graduate), “Development of educational robotics lessons for high school; Application on the Moodle asynchronous learning platform”, 2018.

- Supervision of special topics projects in the CCE/ECE department
- Participation in the translation into Greek of the book “Computer Architecture: A quantitative approach” of J.Hennessy and D.Patterson
- Review for the Journal ACM Transactions on Architecture and Compiler Optimizations (TACO)

HONORED DISTINCTIONS:

- Fellowships from the State Fellowship Foundation (during my undergraduate studies at NTUA)
- Fellowship from the A.Onassis Foundation (after my undergraduate studies, declined)
- Research and Teaching Assistantships (during my graduate studies at UIUC)
  - Research assistant (Fall 1989 - Spring 1999)
  - Teaching assistant (Fall 1996)

FOREIGN LANGUAGES:

- English (excellent due to a PhD degree in the USA).
- German («Kleines Deutsches Sprachdiplom» degree).

PUBLICATIONS:

THESES-BOOKS

MSThesis. Simulation of Static and Dynamic Task Scheduling on Multiprocessor Systems, University of Illinois.

PhDThesis. Loop Scheduling for Multithreaded Processors, University of Illinois.

A. JOURNALS

A1. G.Papakonstantinou, T.Panayiotopoulos, G.Dimitriou, "AGP: A Parallel Processor for Knowledge and Software Engineering", The Computer Journal, Vol.35, 1992, pp. A193-199, Oxford University Press.

A2. G.Dimitriou, A.Tziouvaras, "A Functional Unit Network for Rapid, Low-Power Loop Execution", International Journal of Innovation and Regional Development, special issue on: "Information and Communication Technologies Research and Applications in South East Europe", Vol.6 No.3, 2015, pp. 267-284, Inderscience Publishers.

A3. M.Dossis, V.Hados, G.Dimitriou, "Automatic Generation of Trigonometric Hardware with HLS Tools Using the CubedC Hardware Compiler/Optimizer", International Journal of Engineering Researches and Management Studies, Vol.1 No.1, 2014, pp.15-25.

A4. M.Dossis, G.Dimitriou, "Are HLS Tools Healthy?", Engineering, Technology & Applied Science Research, Vol.5, No.2, 2015, pp.790-794.

B. CONFERENCES

B1. G.Dimitriou, P.Tsanakas, G.Papakonstantinou, "The Multi-Transputer Implementation of a Hierarchical Edge Detection Algorithm", IMACS/IFAC Int. Symposium on Parallel and Distributed Computing in Engineering Systems, 1991.

B2. G.Dimitriou, C.D.Polychronopoulos, "Loop Scheduling for Multithreaded Processors", IEEE Int. Conference on Parallel Computing in Electrical Engineering – PARELEC, 2004.

B3. G.Dimitriou, C.D.Polychronopoulos, "Hardware Support for Multithreaded Execution of Loops with Limited Parallelism", 10th Panhellenic Conference on Informatics – PCI, 2005. Also in LNCS 3746, Advances in Informatics, pp. 622-632, Springer Verlag.

B4. G.Dimitriou, P.K.Kikiras, G.I.Stamoulis, I.N.Avaritsiotis, "A Tool for Calculating Energy Consumption in Wireless Sensor Networks", 10th Panhellenic Conference on Informatics – PCI, 2005. Also in LNCS 3746, Advances in Informatics, pp. 611-621, Springer Verlag.

B5. A.Tziouvaras, G.Dimitriou, "Rapid, Low-power Loop Execution in a Network of Functional Units", 17th Panhellenic Conference on Informatics – PCI, 2013.

B6. M.Dossis, V.Hados, G.Dimitriou, "Numerical Block High-Level Synthesis", CSCESM'2014, December 2014.

B7. G.Floros, G.Dimitriou, G.Stamoulis, "Electromigration: Estimation methodology for the sub-45nm era", CSCESM'2014, December 2014.

B8. A.Dadaliaris, G.Dimitriou, G.Stamoulis, "VDA-Place: Voltage-Drop-Aware Standard Cell Placement", CSCESM'2014, December 2014.

B9. S.Ioannidis, D.Ntioudis, C.Antoniadis, A.Dadaliaris, P.Tsompanopoulou, N.Evmorfopoulos, G.Dimitriou, G.Stamoulis, "Optimization of an Integrated Circuit Placement Algorithm in a Parallel Environment", CSCESM'2014, December 2014.

B10. G.-I.Paliaroutis, P.Tsoumanis, G.Dimitriou, G.Stamoulis, "SER analysis for multiple affected gates", CSCESM'2014, December 2014.

B11. M.Zervas, M.Spanou, G.Dimitriou, G.Stamoulis, "Compact Physical Model of TSV for quick and accurate exploration of 3DICs", CSCESM'2014, December 2014.

B12. M.Dossis, V.Hados, G.Dimitriou, "Hardware Trigonometry with High-level Synthesis Using the CubedC Hardware Compiler/Optimizer", QUAESTI-Virtual Multidisciplinary Conference, December 2014.

B13. G.Dimitriou, M.Dossis, "Experimenting with a High-Level Synthesis System Front End", PACET'2015, May 2015. Proceedings to appear in the Journal of Engineering Science and Technology Review.

B14. A.Dadaliaris, P.Oikonomou, G.Dimitriou, G.Stamoulis, "VDA Place+: Voltage-Drop-Aware Placement", PACET'2015, May 2015. Proceedings to appear in the Journal of Engineering Science and Technology Review.

B15. T.Strousidou, C.Antoniadis, I.Arvanitakis, G.Dimitriou, N.Evmorfopoulos, P.Tsompanopoulou, P.Bozanis, G.Stamoulis, "Accelerating GORDIAN-Based Placement through Null Space Removal Techniques", PACET'2015, May 2015. Proceedings to appear in the Journal of Engineering Science and Technology Review.

B16. G.-I.Paliaroutis, P.Tsoumanis, G.Dimitriou, G.Stamoulis, "SER Analysis for Multiple Affected Gates", PACET'2015, May 2015. Proceedings to appear in the Journal of Engineering Science and Technology Review.

B17. M.Dossis, G.Dimitriou, "Evaluating MPEG2 through High-level Synthesis Tools", 3rd International Virtual Conference on Advanced Scientific Results, May 2015.

B18. D.Ntioudis, C.Kalonakis, P.Giannakou, C.Antoniadis, G.Stamoulis, P.Tsompanopoulou, N.Evmorfopoulos, J.Moondanos, G.Dimitriou, "CCSOpt: A Continuous Gate-Level Resizing Tool", 4th International Conference on Modern Circuits and Systems Technology – MOCAST, May 2015.

B19. P.Giannakou, C.Antoniadis, C.Kalonakis, D.Ntioudis, G.Stamoulis, P.Tsompanopoulou, N.Evmorfopoulos, J.Moondanos, G.Dimitriou, "GDS2trim: Physical Layout Manipulation Utility for continuous transistor sizing", 4th International Conference on Modern Circuits and Systems Technology – MOCAST, May 2015.

B20. K.Kalaitzidis, G.Dimitriou, G.Stamoulis, M.Dossis, "Performance and Power Simulation of a Functional-Unit-Network Processor with Simplescalar and Wattch", 19th Panhellenic Conference on Informatics – PCI, October 2015.

B21. M.Dossis, G.Dimitriou, "Hardware Synthesis of High-Level C Constructs", 19th Panhellenic Conference on Informatics – PCI, October 2015.

B22. G.Chatzianastasiou, A.Tsakyridis, G.Dimitriou, M.Dossis, "Compiler Transformations in Hardware Synthesis of Mpeg2 Codes", IEEE International Conference on Modern Circuits and Systems Technology – MOCAST, May 2016.

B23. G.-I.Paliaroutis, P.Tsoumanis, G.Dimitriou, G.Stamoulis, "SER Analysis of Multiple Transient Faults in Combinational Logic", South-East Europe Design Automation, Computer Engineering, Computer Networks and Social Media Conference – SEEDA-CECNSM, September 2016.

B24. G.Dimitriou, G.Chatzianastasiou, A.Tsakyridis, G.Stamoulis, M.Dossis, "Source-Level Compiler Optimizations for High-Level Synthesis", South-East Europe Design Automation, Computer Engineering, Computer Networks and Social Media Conference – SEEDA-CECNSM, September 2016.

B25. G.Dimitriou, M.Dossis, G.Stamoulis, "Loop Pipelining in High-Level Synthesis with CCC", IEEE International Conference on Modern Circuits and Systems Technology – MOCAST, May 2017.

B26. G.Dimitriou, M.Dossis, G.Stamoulis, "Minimal-Area Loop Pipelining for High-Level Synthesis with CCC", South-East Europe Design Automation, Computer Engineering, Computer Networks and Social Media Conference – SEEDA-CECNSM, September 2017.

B27. M.Dossis, G.Dimitriou, "Resolving Loop Pipelining Issues in the CCC High-level Synthesis E-CAD Framework", 41st International Conference on Telecommunications and Signal Processing – TSP, July 2018.

B28. G.Dimitriou, M.Dossis, G.Stamoulis, "Operation Dependencies in Loop Pipelining for High-Level Synthesis", South-East Europe Design Automation, Computer Engineering, Computer Networks and Social Media Conference – SEEDA-CECNSM, September 2018.

B29. G.-I.Paliaroutis, P.Tsoumanis, N.Evmorfopoulos, G.Dimitriou, G.Stamoulis, "A Placement-aware Soft Error Rate Estimation of Combinational Circuits for Multiple Transient Faults in CMOS Technology", 31st IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems - DFT, October 2018.

B30. D.Varsos, G.Dimitriou, "Development of Educational Robotics e-Lessons for High-School; Implementation on the Asynchronous e-Learning Moodle Platform", 4th International Conference for the Promotion of Educational Innovation, October 2018.

B31. G.I.Paliaroutis, P.Tsoumanis, N.Evmorfopoulos, G.Dimitriou, G.Stamoulis, "Multiple Transient Faults in Combinational Logic with Placement Considerations", IEEE International Conference on Modern Circuits and Systems Technology – MOCAST, May 2019.

B32. A.Tziouvaras, G.Dimitriou, M.Dossis, G.Stamoulis, "Instruction-Based Timing Analysis in Pipelined Processors", South-East Europe Design Automation, Computer Engineering, Computer Networks and Social Media Conference – SEEDA-CECNSM, September 2019.

B33. A.Tziouvaras, G.Dimitriou, M.Dossis, G.Stamoulis, "Instruction-Flow-Based Timing Analysis in Pipelined Processors", PAnhellenic Conference on Electronics & Telecommunications – PACET, November 2019, Volos, to be presented.